In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Currently amended) A process for deterministic transmission of asynchronous data in packets issued by acquisition and processing systems in the field of data acquisition and telemetry of testing installations, in which data arriving asynchronously is stored in buffers as it arrives and then transmitted within a delay not exceeding a time TT, said process comprising the following steps:

receiving data contained in a set of said buffers in ~~one or more~~ a plurality of packeting modules;

commencing a first packeting realization cycle of a duration TP in said packeting modules, said packeting realization cycle including, for a first set of packets, start of packeting, packeting with sorting and enhancement of data, end of packeting and sending of packets,

ending, for said first set of packets, said packet realization cycle in said packeting modules at the request of a message composition module configured to receive the outputs of all the packeting modules and to control the packeting cycle;

forwarding to said message composition module said first set of packets regardless of the state of completion of said first packeting realization cycle, such that the condition TP = TT is substantially met when TMS << TP, with TMS being transmission time;

commencing a second packeting realization cycle for a second set of packets;

recovering one after another the first set of packets, in a predefined order, in the message composition module;

setting, in a formatting ~~the message composition~~ module, a first message comprised of the first set of packets to an electrical format in a protocol used for message transmission.

2. (Currently amended) A device for deterministic transmission of asynchronous data in packets issued by acquisition and processing systems in the field of data acquisition and telemetry of testing installations, said device, said transmission occurring within a time delay not exceeding a duration TT, comprising:

~~an~~ at least one input module receiving said data;

~~one or more~~ a plurality of buffers configured to receive digital data from the at least one input module;

a plurality of packeting modules connected to said ~~one or more~~ buffers;

at the least one control module for buffer dump monitored by at least one packeting module of said plurality of packeting modules;

a message composition module receiving the outputs of said plurality of packeting modules for composing a message therefrom, said message composition module configured to control the packeting cycle in sending ~~send~~ to each of said plurality of packeting modules an order to terminate a packet assembly procedure regardless of whether said packet assembly procedure is completed such that the condition TT = TP is met when TMS << TP, wherein TP is a packeting time and TMS is a transmission time;

a packet formatting module configured to format said message from said message composition module; and

an output module configured to transmit said message on a transmission line.

3. (Previously presented) The process of claim 1, further comprising conducting data acquisition and real-time processing for test installations of new aeroplanes.